



LM73605 SIMPLE SWITCHER® 3.5 V to 36 V, 5 A Synchronous Step-Down Voltage Converter

1 Features

- High efficiency at light load architecture (PFM)
- Synchronous rectification
- Adjustable frequency range of 350 kHz - 2.2 MHz (500 kHz default)
- Frequency synchronization to external clock
- Forced PWM Capability
- Internal compensation
- Stable with many combinations of ceramic, polymer, tantalum, and aluminum capacitors
- Power good flag
- Soft-start into pre-biased load
- Output voltage tracking capability
- Precision enable to program system UVLO
- Adjustable soft-start time > 5 ms
- Short circuit protection with 40 ms hiccup mode
- Over temperature thermal shutdown protection
- Output current range: 0 A to 5 A
- Input voltage range: 3.5 V to 36 V
- Output voltage range: 1.0 V to 95% of VIN
- 3 μ A quiescent current in shutdown
- 15 μ A quiescent current switching

2 Applications

- Industrial distributed power application
- Automotive systems
- Telecommunications systems
- General purpose wide VIN regulation

3 Description

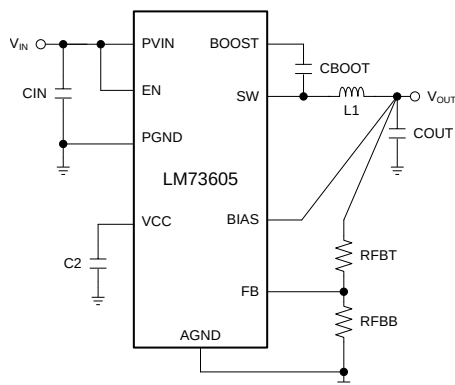
The LM73605 SIMPLE SWITCHER® regulator is an easy to use synchronous step-down DC-DC converter capable of driving up to 5 A of load current from an input of up to 36 V. The LM73605 provides exceptional efficiency and output accuracy in a very small solution size. Peak current mode control is employed. Additional features such as adjustable switching frequency, synchronization, power good flag, precision enable, adjustable soft-start, and tracking provide both a flexible and easy to use solution for a wide range of applications. Automatic frequency fold-back at light load improves light load efficiency. The family requires few external components and has a pin out designed for simple, optimum PCB layout. Protection features include thermal shutdown, input under-voltage lockout, cycle-by-cycle current limit, and short-circuit protection. The LM73605 device is available in a QFN 30 pin leadless package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM73605	QFN (30) Wettable Flanks	6.00 mm x 4.0 mm x 0.8 mm 0.5 mm lead pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current (5 Vout, 500 kHz, AUTO, L = 3.3 μ H)

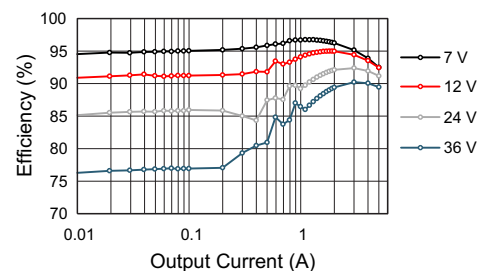


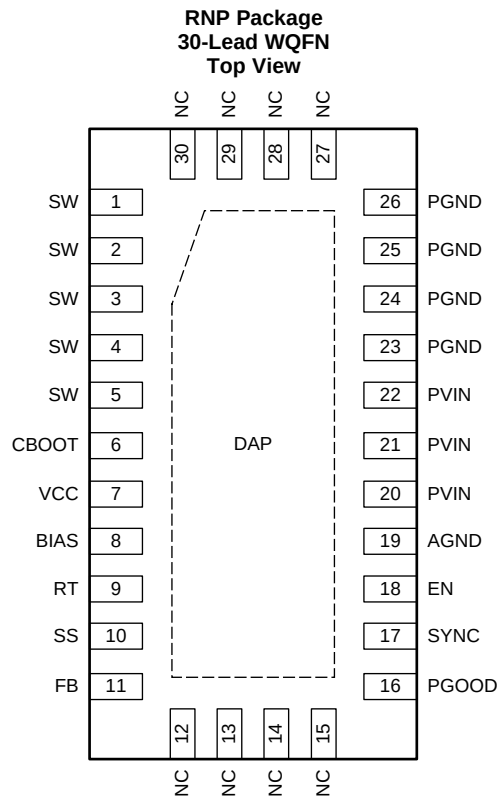
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4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
SW	1-5	P	Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to power inductor.
CBOOT	6	P	Boot-strap capacitor connection for high-side driver. Connect a high quality 470 nF capacitor from this pin to the SW pin.
VCC	7	P	Output of internal bias supply. Used as supply to internal control circuits. Connect a high quality 1.0 μ F capacitor from this pin to GND. This pin can supply up to 10 mA of current to external loads.
BIAS	8	P	Optional BIAS LDO supply input. Recommend to tie to V_{OUT} when $3.3\text{ V} \leq V_{OUT} \leq 30\text{V}$, or tie to an external 3.3 V or 5 V rail if available, to improve efficiency. When used, place a 1 μ F capacitor from this terminal to ground. Tie to ground when not in use.
RT	9	A	Switching frequency adjustment. Place a resistor from this pin to GND to set the switching frequency. If grounded the default switching frequency will be 500 kHz. See detailed description in Applications section.
SS/TRK	10	A	Soft start pin. Internal soft start is set for 5 ms. Leave this pin floating to use the internal soft start. A 2 μ A current sourced from this pin can charge an external capacitor to create a longer soft start time. For example a 22 nF capacitor will extend the soft start time to approximately 11 ms. Connect external ramp for tracking.
FB	11	A	Feedback input to regulator. Connect to output voltage node for fixed 5 V and 3.3 V options. To create an adjustable output voltage, connect a resistor divider using the equations in the Applications section. Never short this terminal to ground during operation.
NC	12-15, 27-30	O	Not internally connected. Connect to ground copper shape to improve heat-sinking of the device and board level reliability. See Layout Recommendations.
PGOOD	16	I	Open drain power good flag output. Connect to suitable voltage supply through a current limiting resistor. High = regulator OK, Low = regulator fault. Will go low when EN = low. See detailed description.

(1) A = Analog, O = Output, I = Input, G = Ground, P = Power

Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
SYNC	17	I	Synchronization input to regulator. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock. When used the device will function in forced PWM and disable the PFM light load efficiency mode. When pulled to a logic voltage; High = forced PWM, Low = PFM under Light Loads to improve efficiency. Do not float, if not used connect to ground. See detailed description.
EN	18	I	Precision enable input to regulator. High = on, Low = off. Can be connected to Vin. Precision enable allows the pin to be used as an adjustable UVLO. See Applications section. Do not float.
AGND	19	G	Analog ground terminal. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground.
VIN	20-22	P	Supply input terminals to internal bias LDO and HS power FET. Connect to input supply and input bypass capacitors C _{IN} . Input bypass capacitors must be directly connected to this pin and PGND.
PGND	23-26	G	Power ground terminal, connected to source of low side power FET internally. Connect to system ground, DAP/EP, AGND, ground side of C _{IN} and C _{OUT} . Path to C _{IN} must be as short as possible.
DAP	EP	G	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

E2E is a trademark of Texas Instruments.

SIMPLE SWITCHER is a registered trademark of Texas Instruments.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM73605QRNPRQ1	PREVIEW	WQFN	RNP	30	3000	TBD	Call TI	Call TI	-40 to 125		
LM73605QRNPTQ1	PREVIEW	WQFN	RNP	30	250	TBD	Call TI	Call TI	-40 to 125		
LM73605RNPR	PREVIEW	WQFN	RNP	30	3000	TBD	Call TI	Call TI	-40 to 125		
LM73605RNPT	PREVIEW	WQFN	RNP	30	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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